

FIG. 1

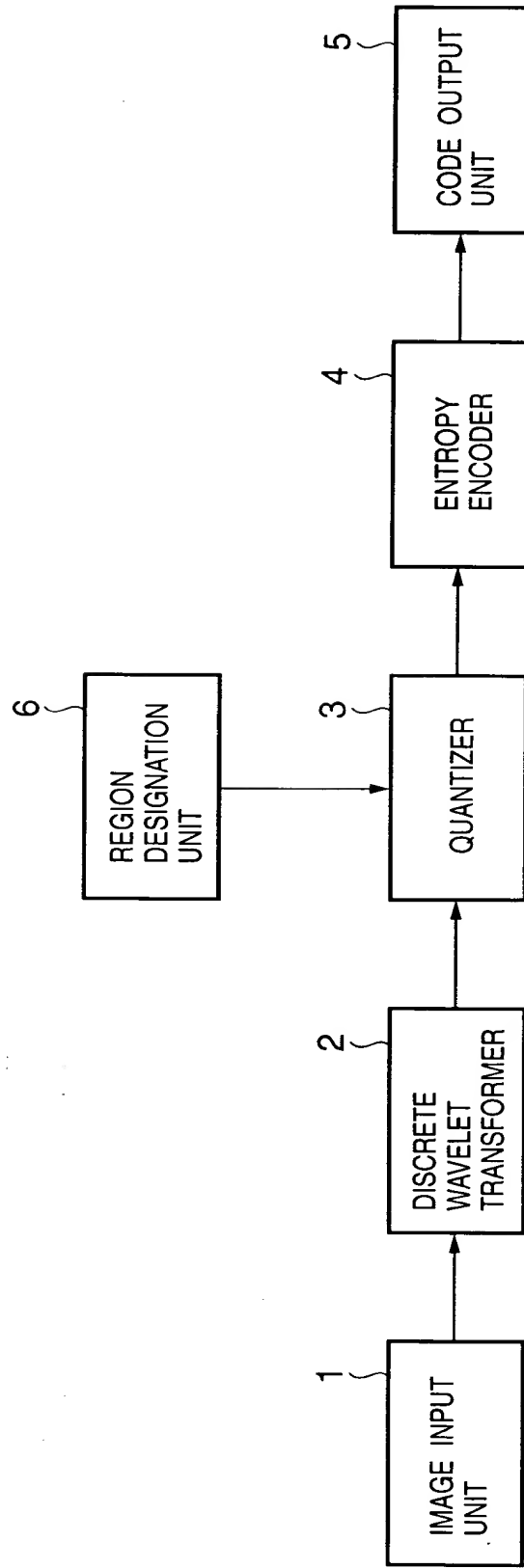


FIG. 2

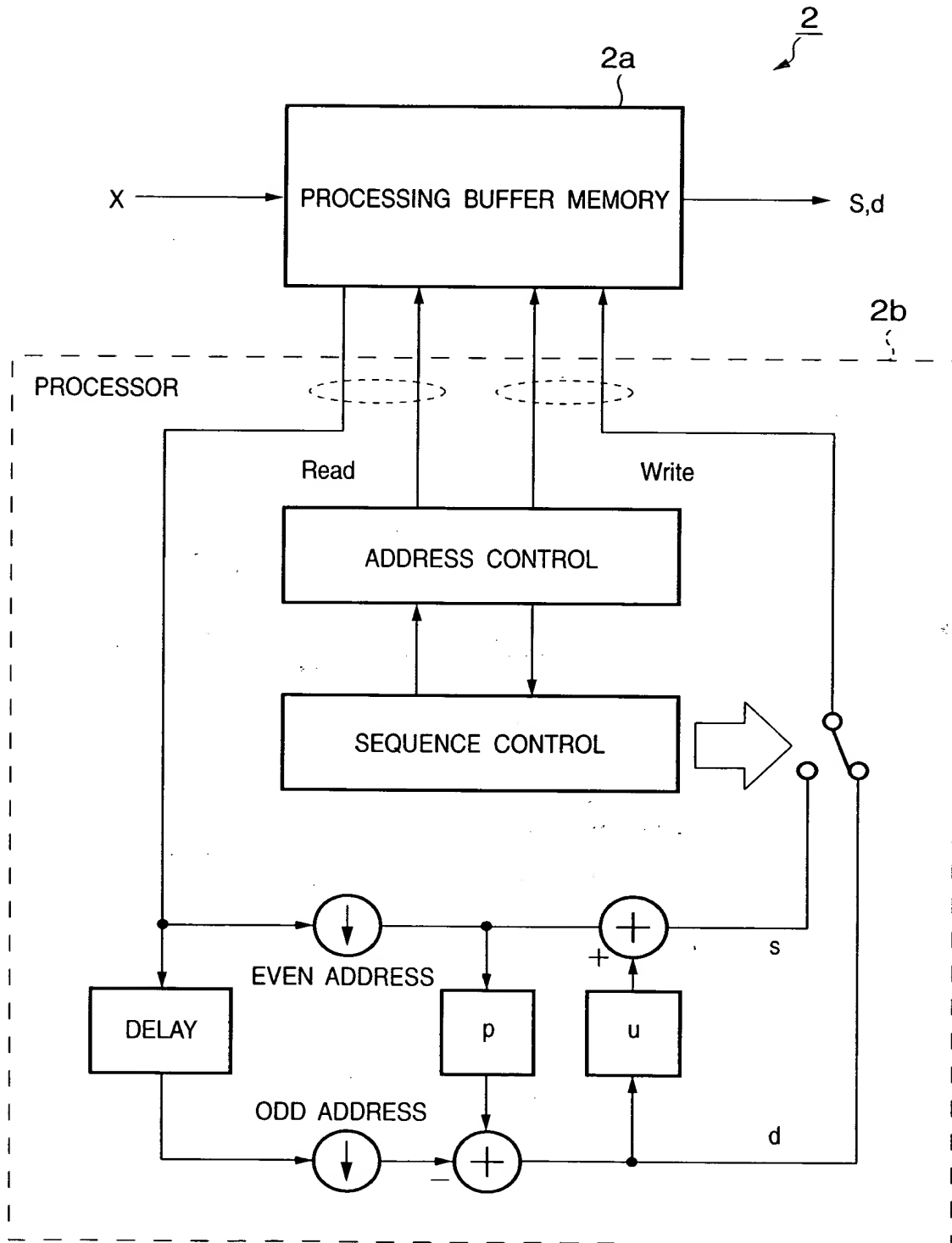


FIG. 3A

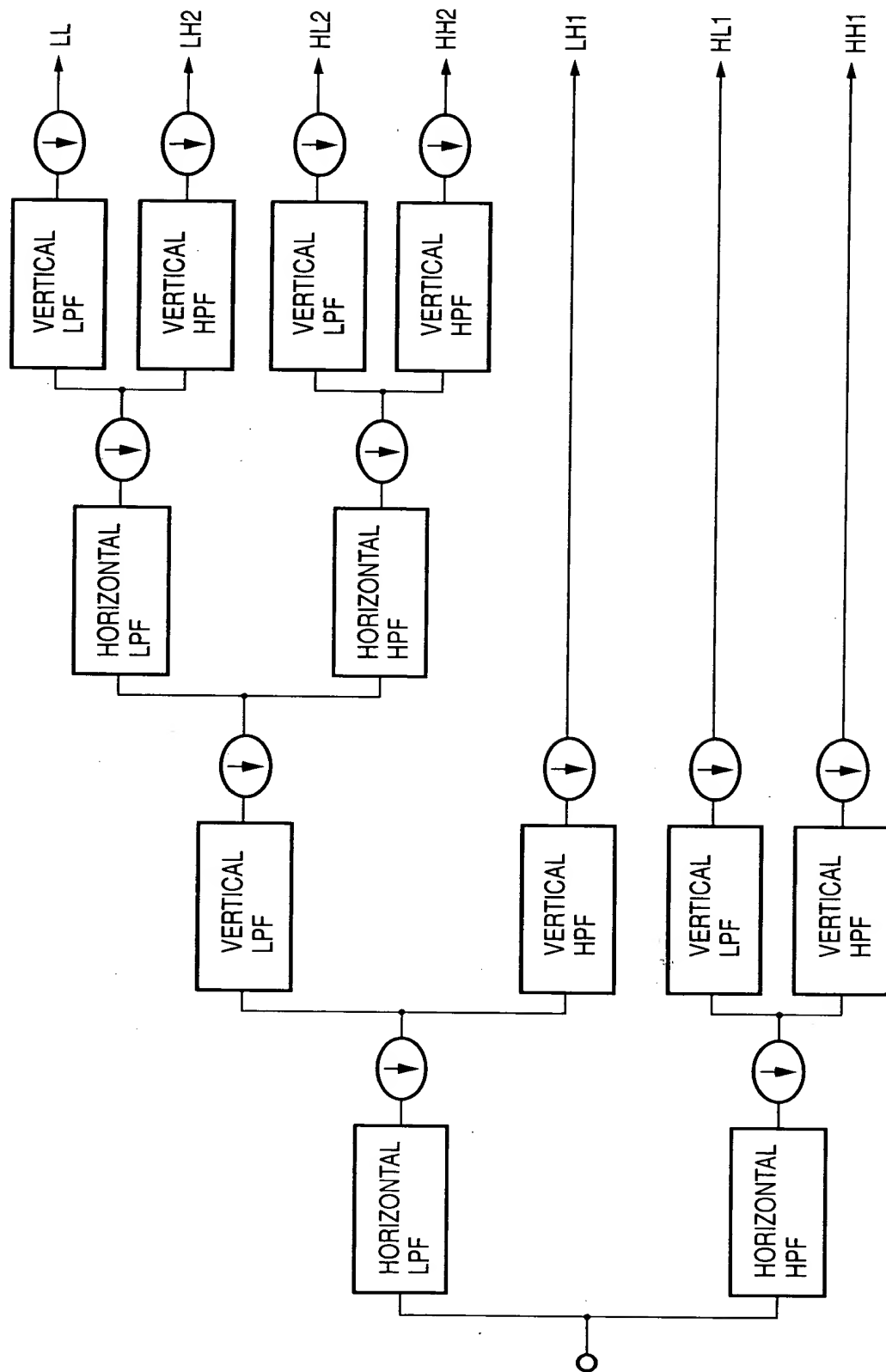


FIG. 3B

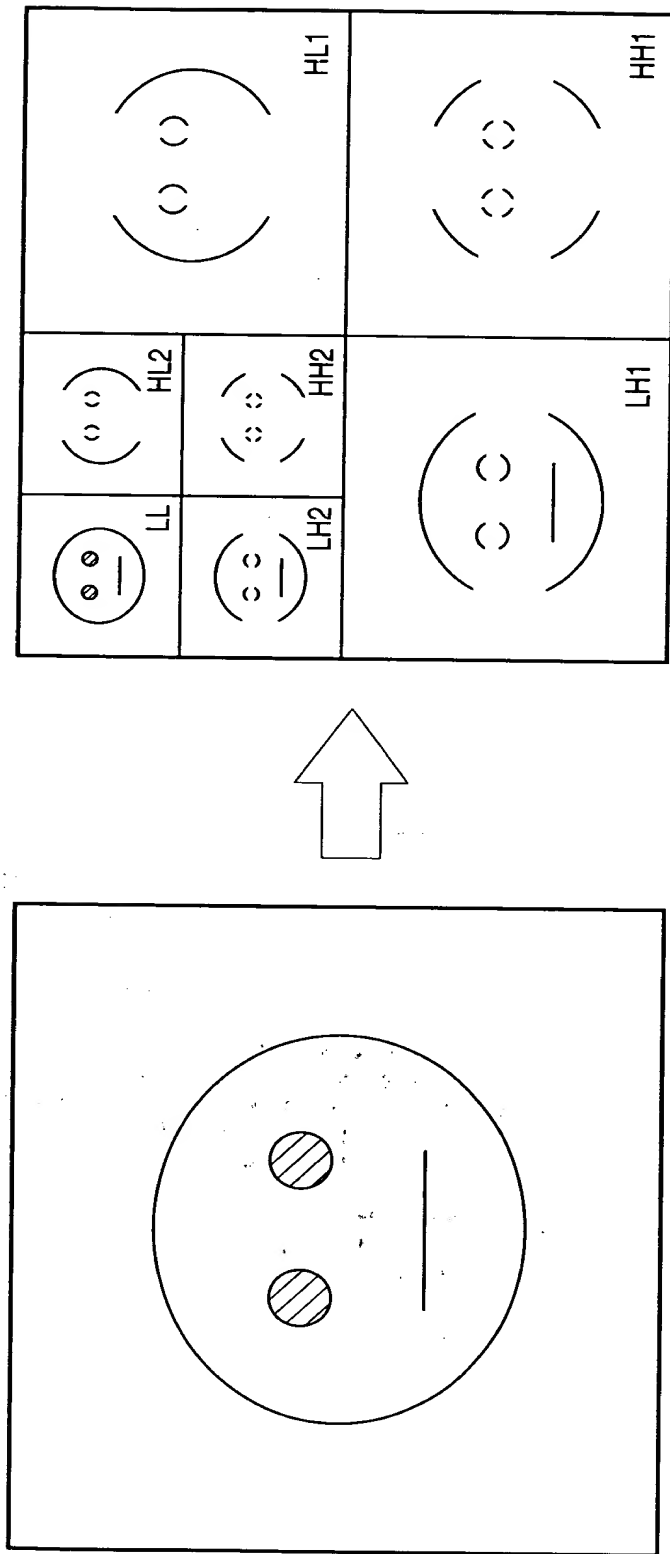


FIG. 4A

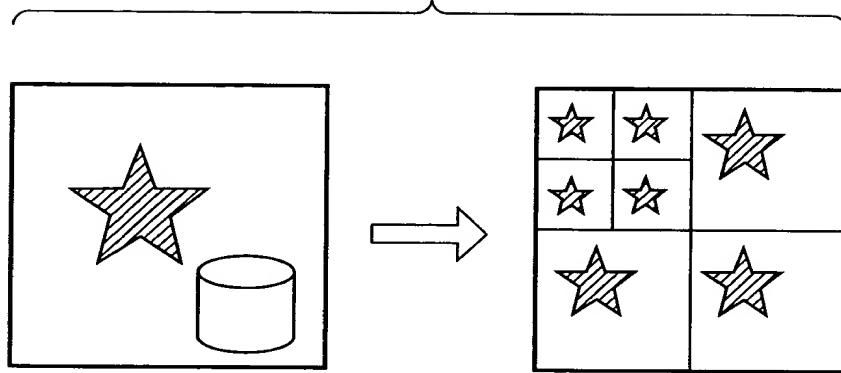


FIG. 4B

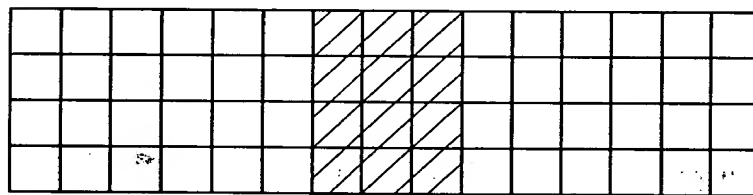


FIG. 4C

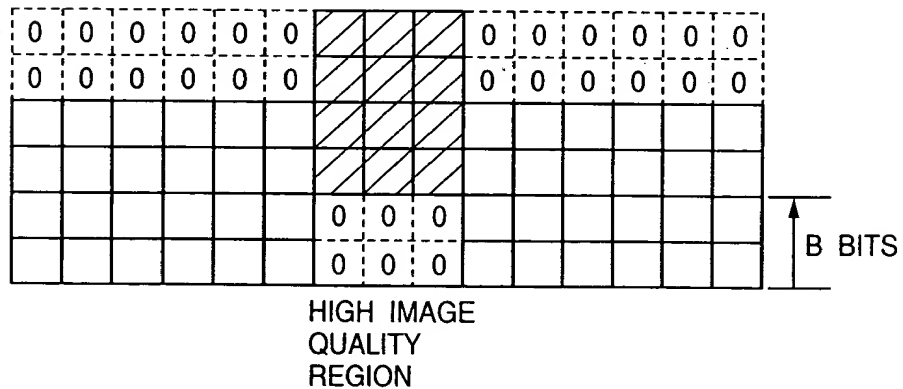


FIG. 5A

FIG. 5B

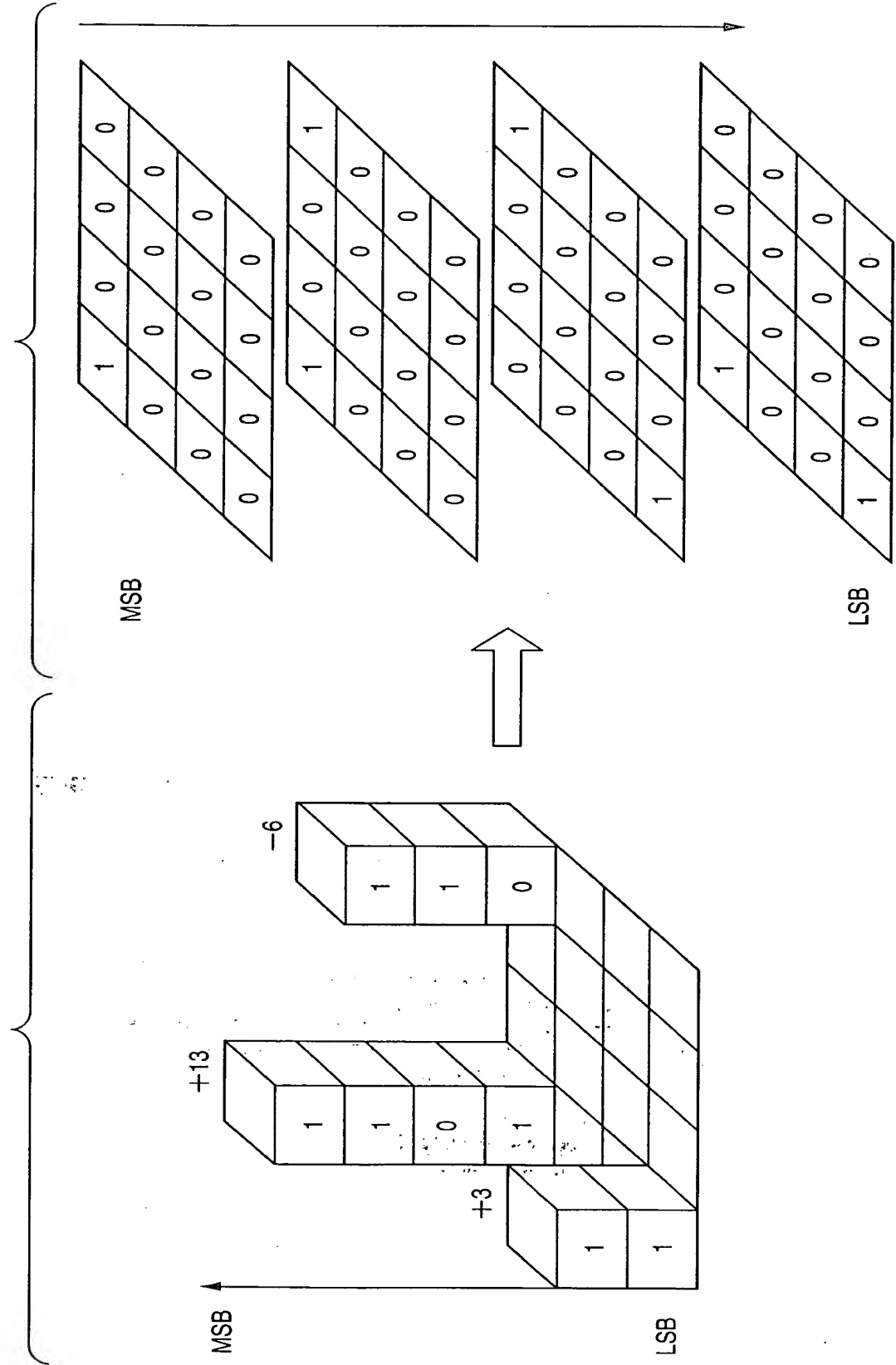


FIG. 6A

RLL	RHL2	RHL1
RLH2	RHH2	
RLH1		RHH1

FIG. 6B

GLL	GHL2	GHL1
GLH2	GHH2	
GLH1		GHH1

FIG. 6C

BLL	BHL2	BHL1
BLH2	BHH2	
BLH1		BHH1

FIG. 7A

YLL	YHL2	YHL1
YLH2	YHH2	
YLH1		YHH1

FIG. 7B

(R-Y) LL	(R-Y) HL2	(R-Y) HL1
(R-Y) LH2	(R-Y) HH2	
(R-Y) LH1		(R-Y) HH1

FIG. 7C

(B-Y) LL	(B-Y) HL2	(B-Y) HL1
(B-Y) LH2	(B-Y) HH2	
(B-Y) LH1		(B-Y) HH1

FIG. 8A

YLL	YHL2	YHL1
YLH2	YHH2	
YLH1		YHH1

FIG. 8B

(R-Y) LL	(R-Y) HL
(R-Y) LH	(R-Y) HH

FIG. 8C

(B-Y) LL	(B-Y) HL
(R-Y) LH	(R-Y) HH

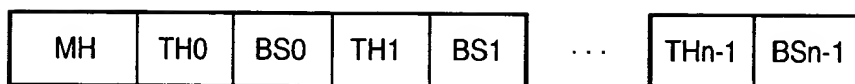
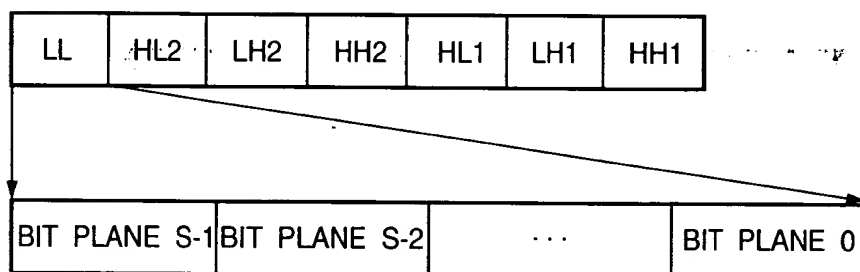
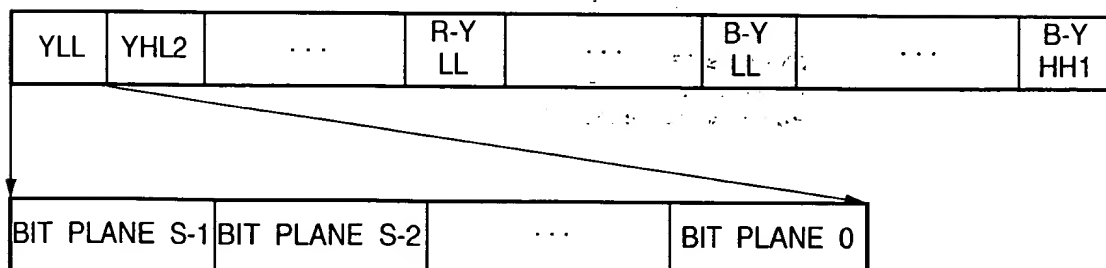
FIG. 9A**FIG. 9B****FIG. 9C****FIG. 9D****FIG. 9E**

FIG. 10A

MH	TH0	BS0	TH1	BS1	...	THn-1	BSn-1
----	-----	-----	-----	-----	-----	-------	-------

FIG. 10B

IMAGE SIZE	TILE SIZE	NUMBER OF COMPONENTS	COMPONENT INFORMATION
---------------	-----------	-------------------------	--------------------------

FIG. 10C

TILE LENGTH	ENCODING PARAMETER	MASK INFORMATION	BIT SHIFT INFORMATION
----------------	-----------------------	---------------------	--------------------------

FIG. 10D

BIT PLANE S-1			BIT PLANE S-2			BIT PLANE 0		
LL	HL2	LH2	LL	...	LL	HL2	LH2	HH2
						HL1	LH1	HH1

FIG. 10E

BIT PLANE S-1				BIT PLANE 0			
YLL	...	YHH2	R-Y LL	...	B-Y HH2	YLL	HL2
						...	YHH1
						R-Y LL	...
						B-Y LL	...
							B-Y HH2

FIG. 11

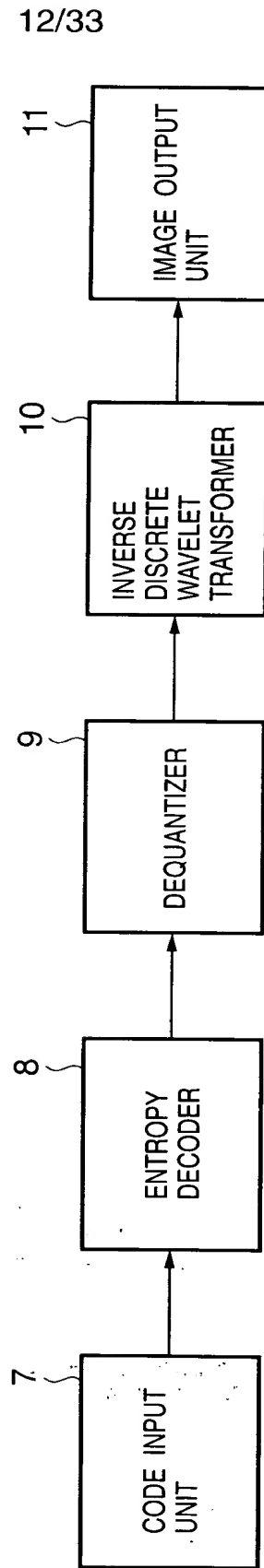


FIG. 12A

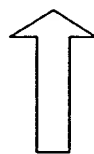
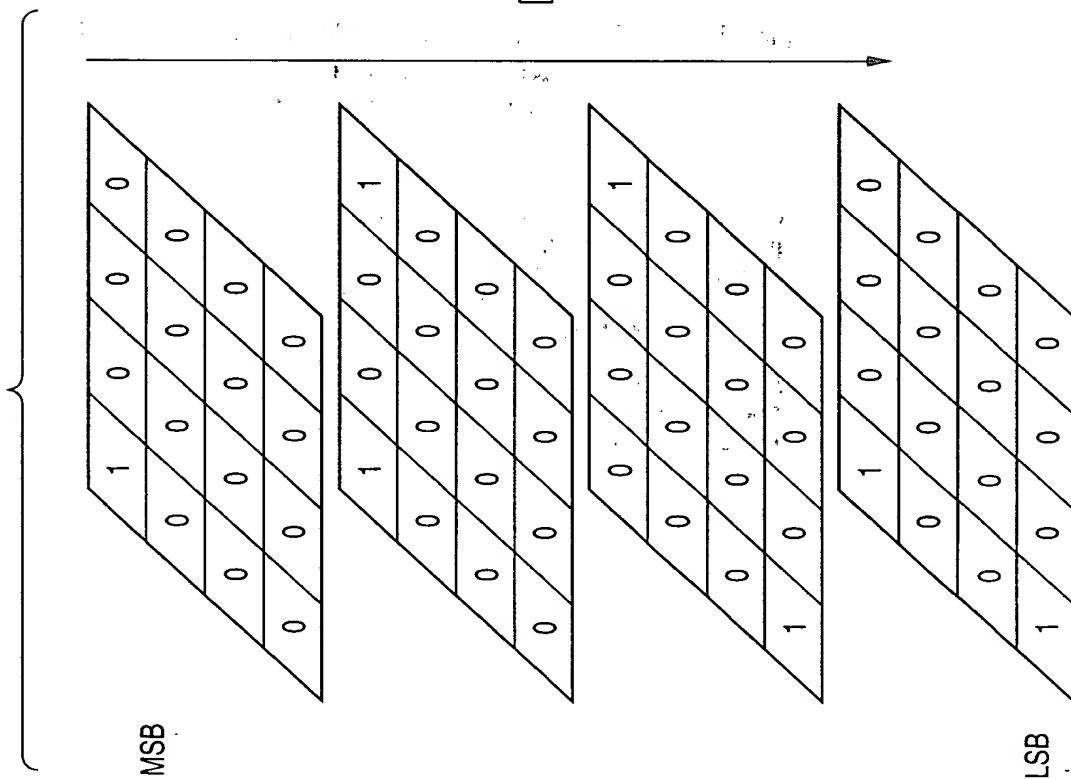


FIG. 12B

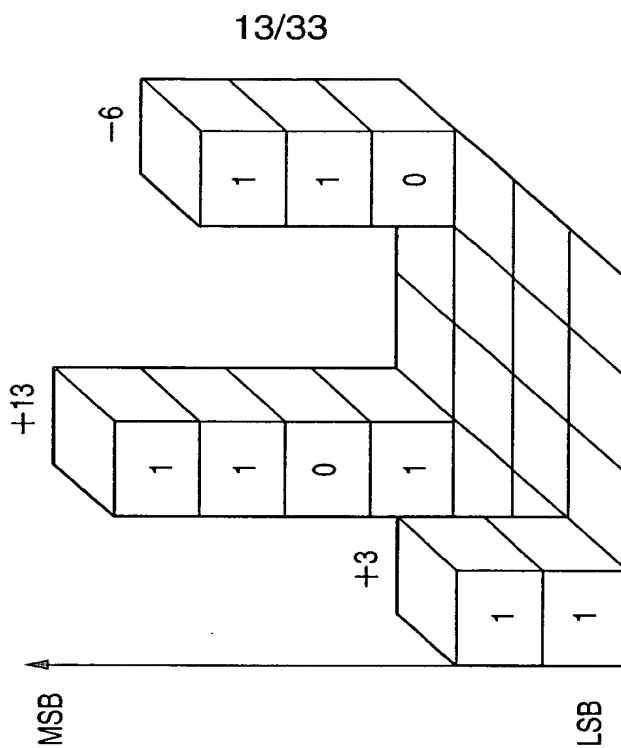


FIG. 13

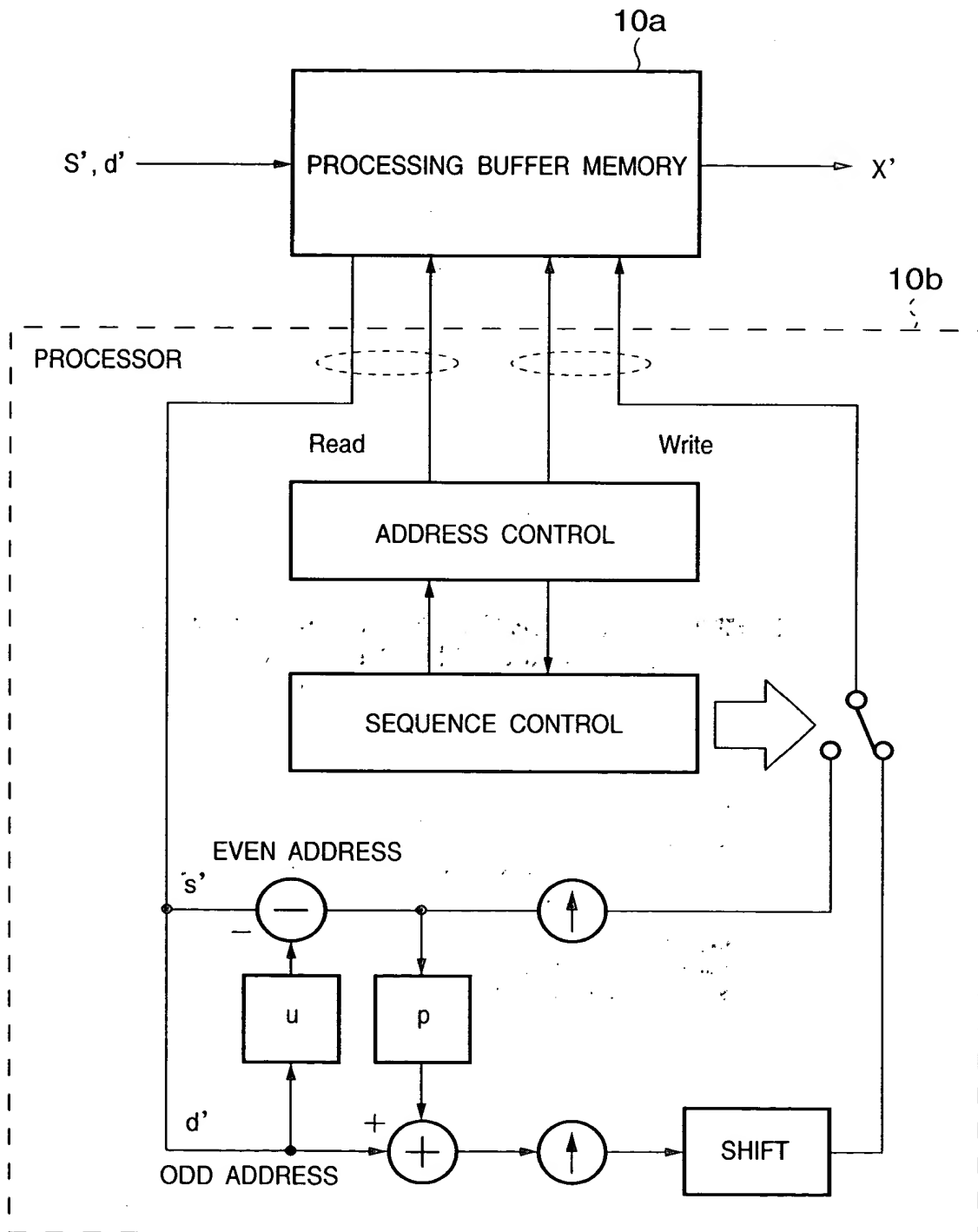


FIG. 14A

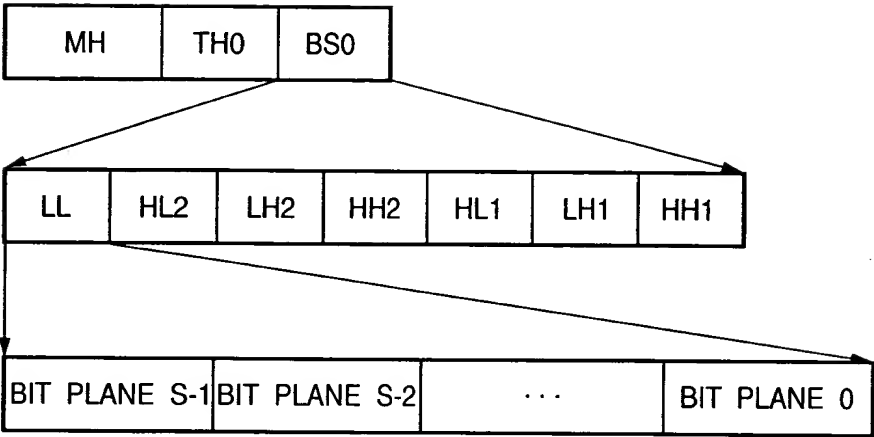
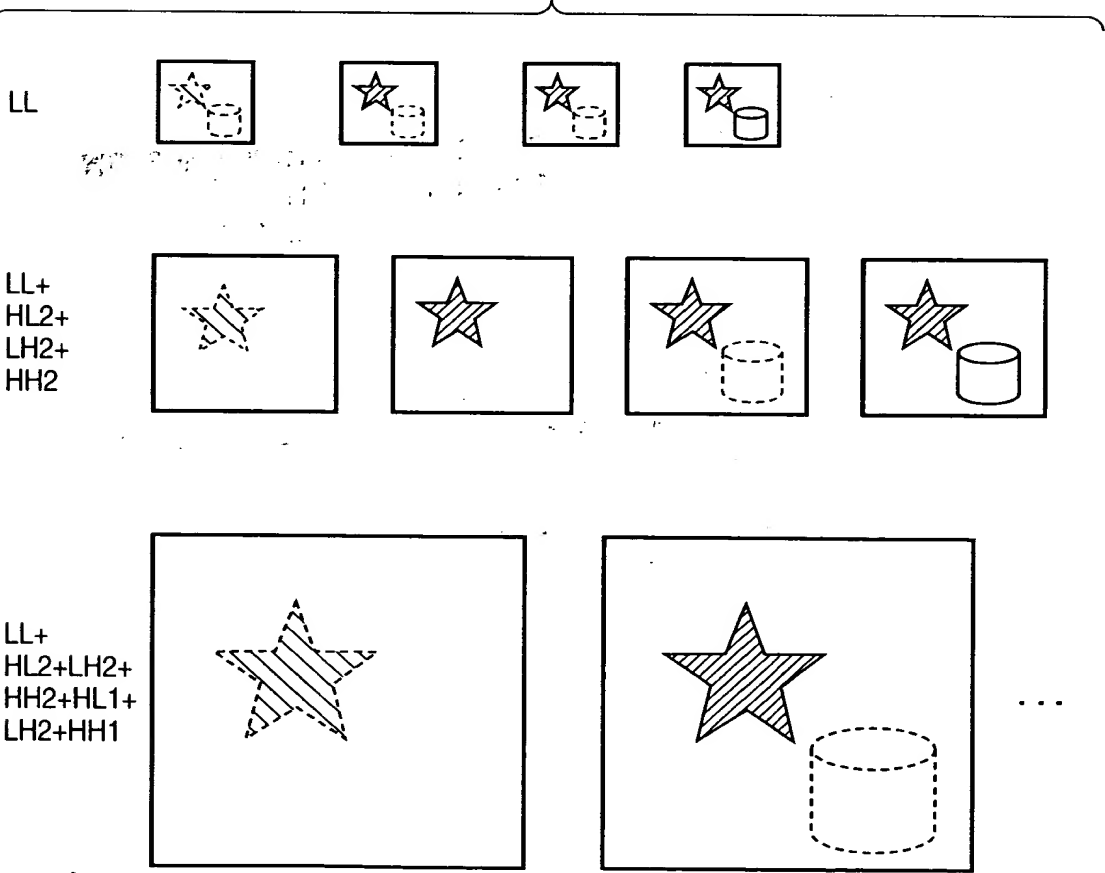


FIG. 14B



The diagram illustrates the mapping of a 4-bit register to a 16-bit bus structure. The register is divided into three fields: MH (Most Significant Half), TH0 (Third Half), and BS0 (Bit Set 0). The bus is divided into three sections: BIT S-1 (4 bits), BIT S-2 (4 bits), and BIT 0 (8 bits). The mapping is as follows:

Register Field	Bus Section	Bit Position	Field Name
MH	BIT S-1	15	LL
		14	HL2
TH0	BIT S-1	13	LH2
		12	LL
BS0	BIT S-2	11	LL
		10	HL2
BS0	BIT S-2	9	LH2
		8	HL2
		7	LH2
		6	HL2
	BIT 0	5	LH1
		4	HL1
		3	LH1
		2	HL1

00892504-062801

FIG. 16A

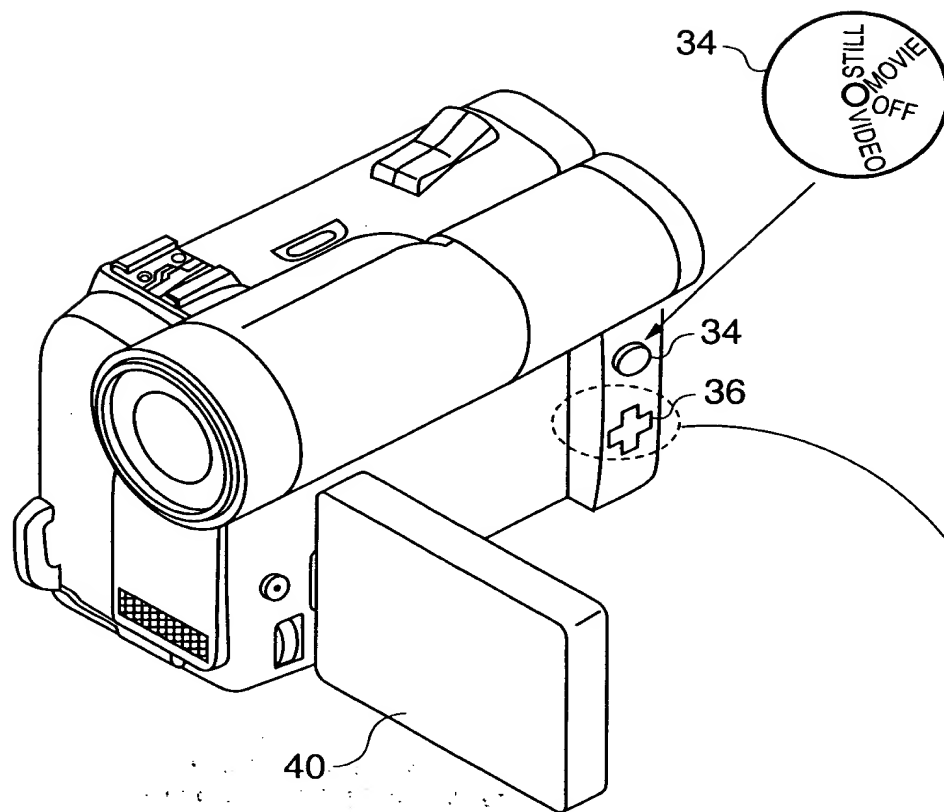


FIG. 16C

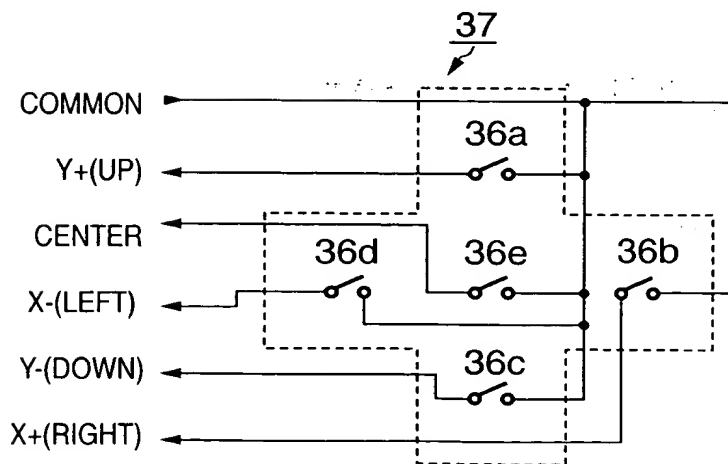
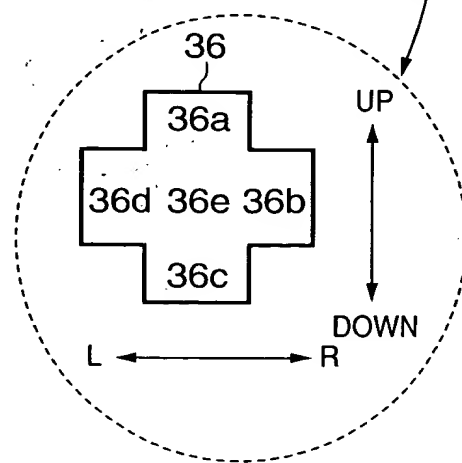


FIG. 16B



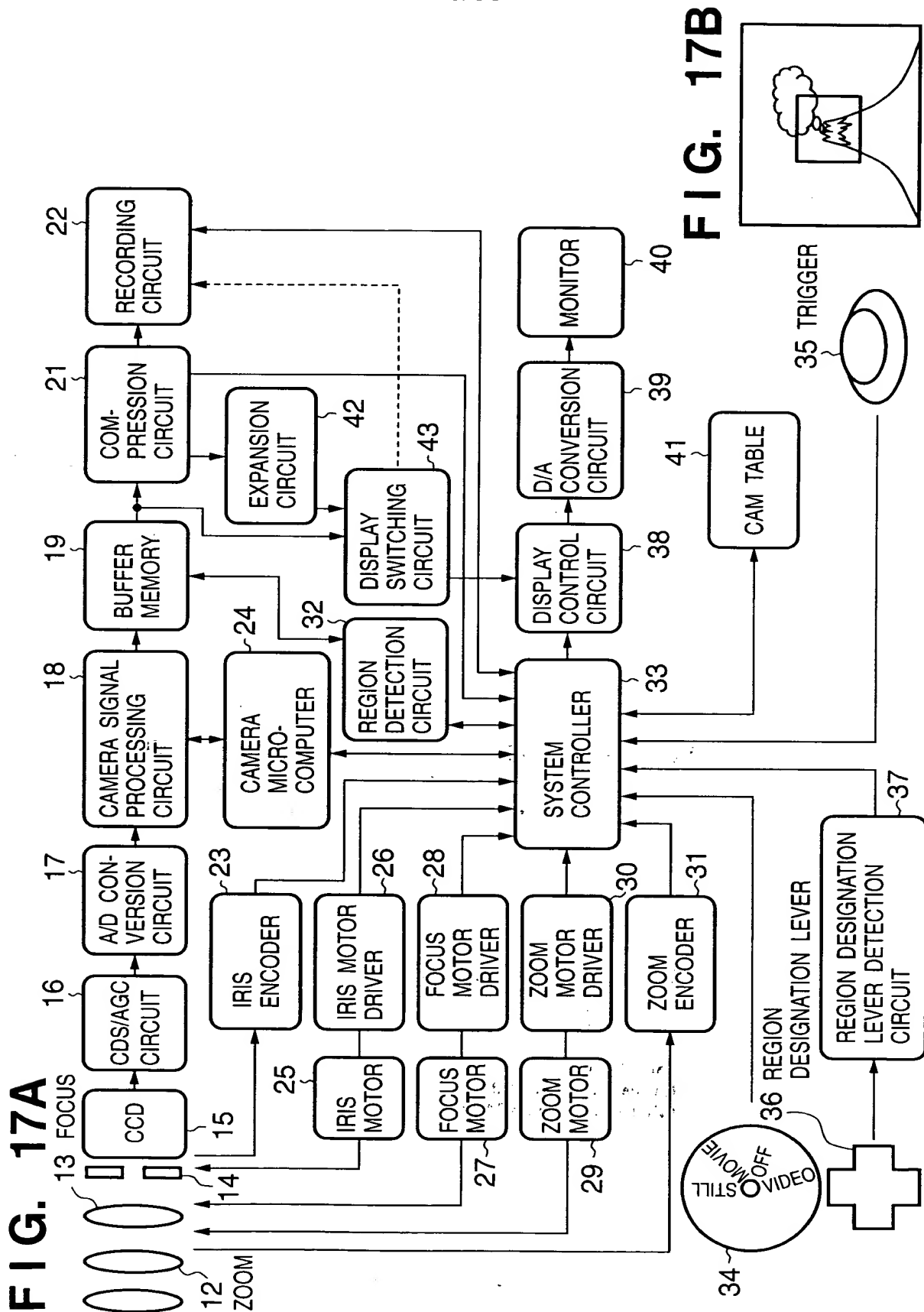


FIG. 17B

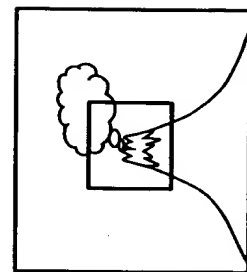


FIG. 18

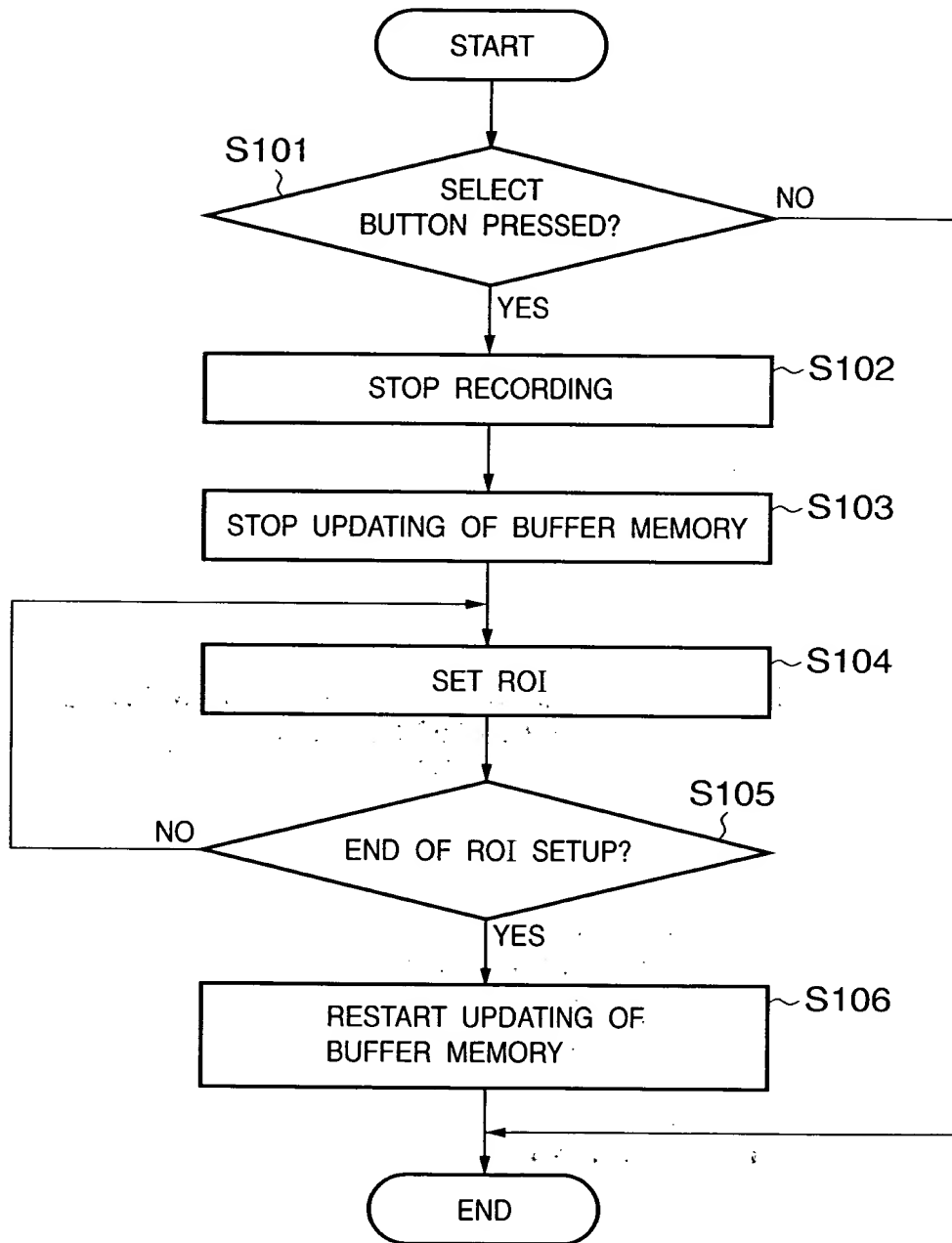


FIG. 19

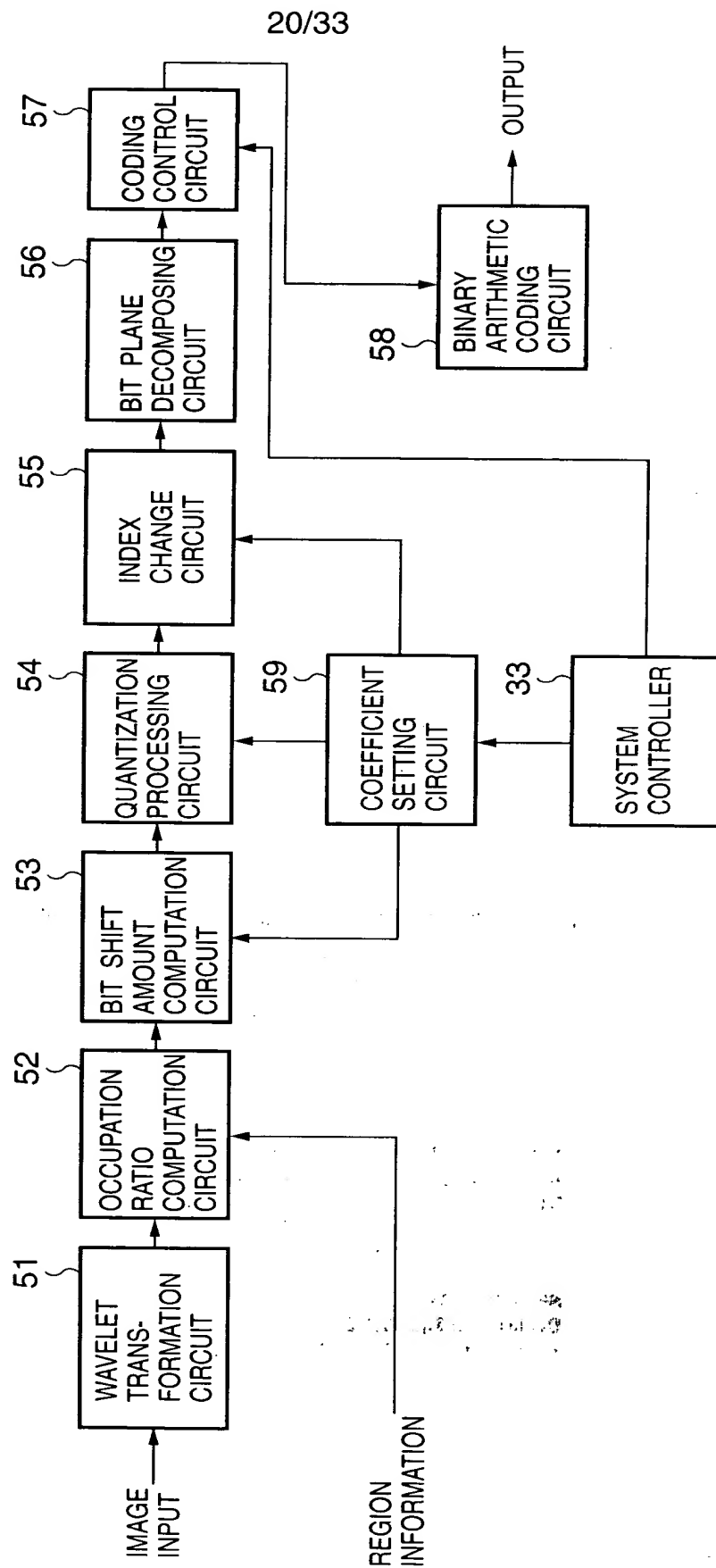


FIG. 20A

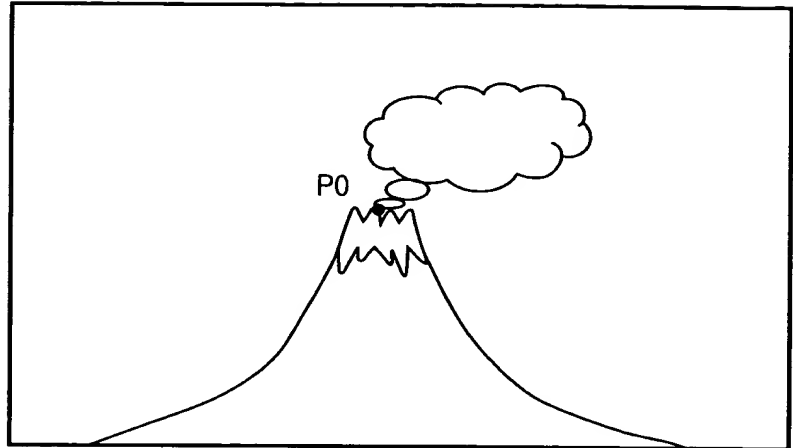


FIG. 20B

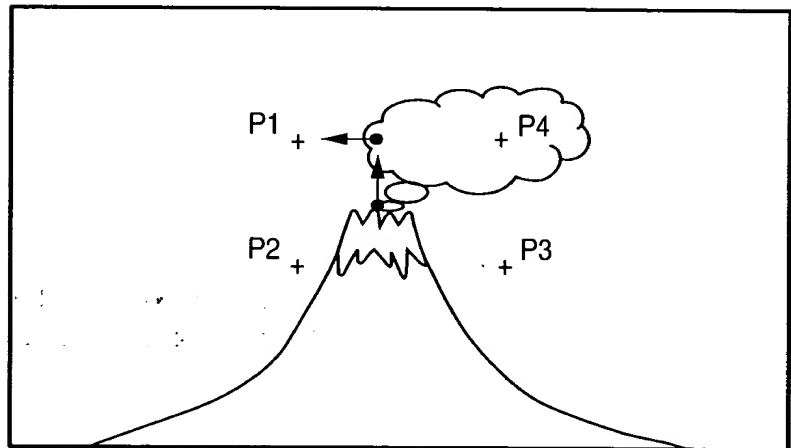
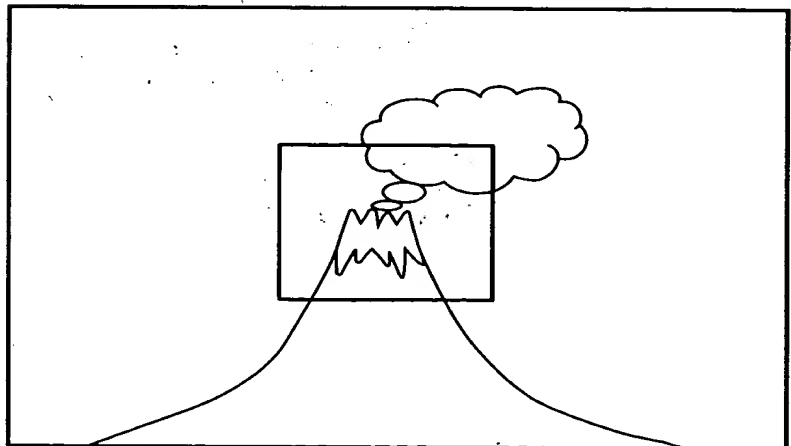


FIG. 20C



00892504-062801

FIG. 21A

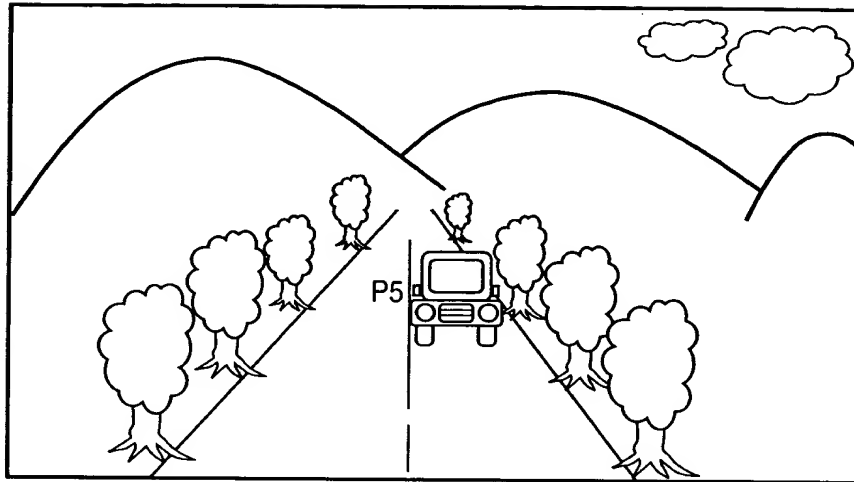


FIG. 21B

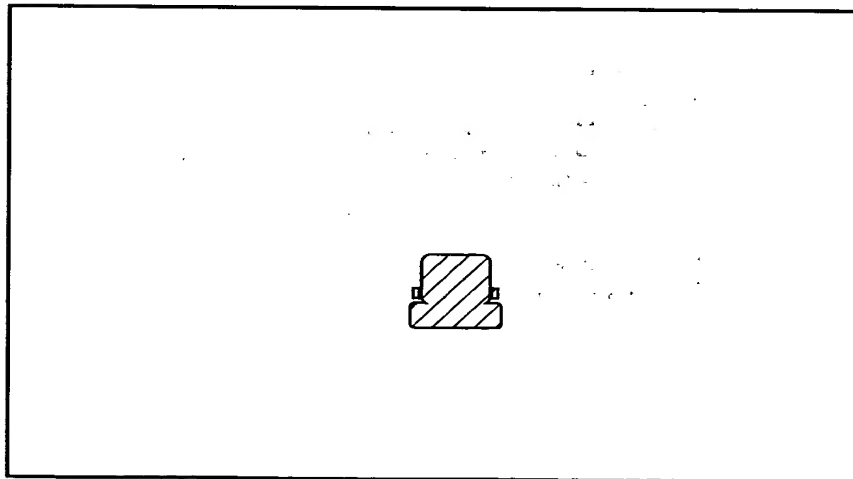


FIG. 22

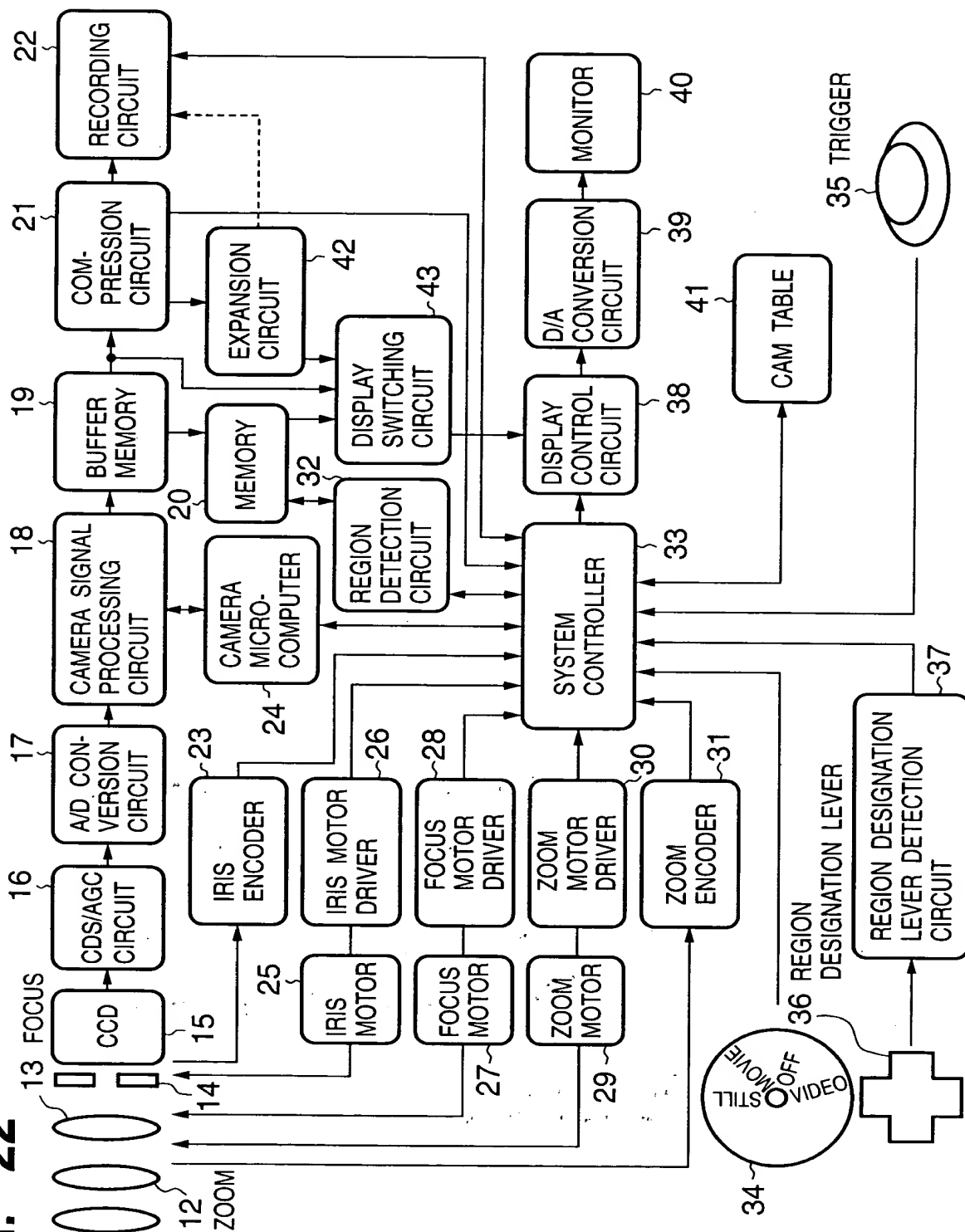
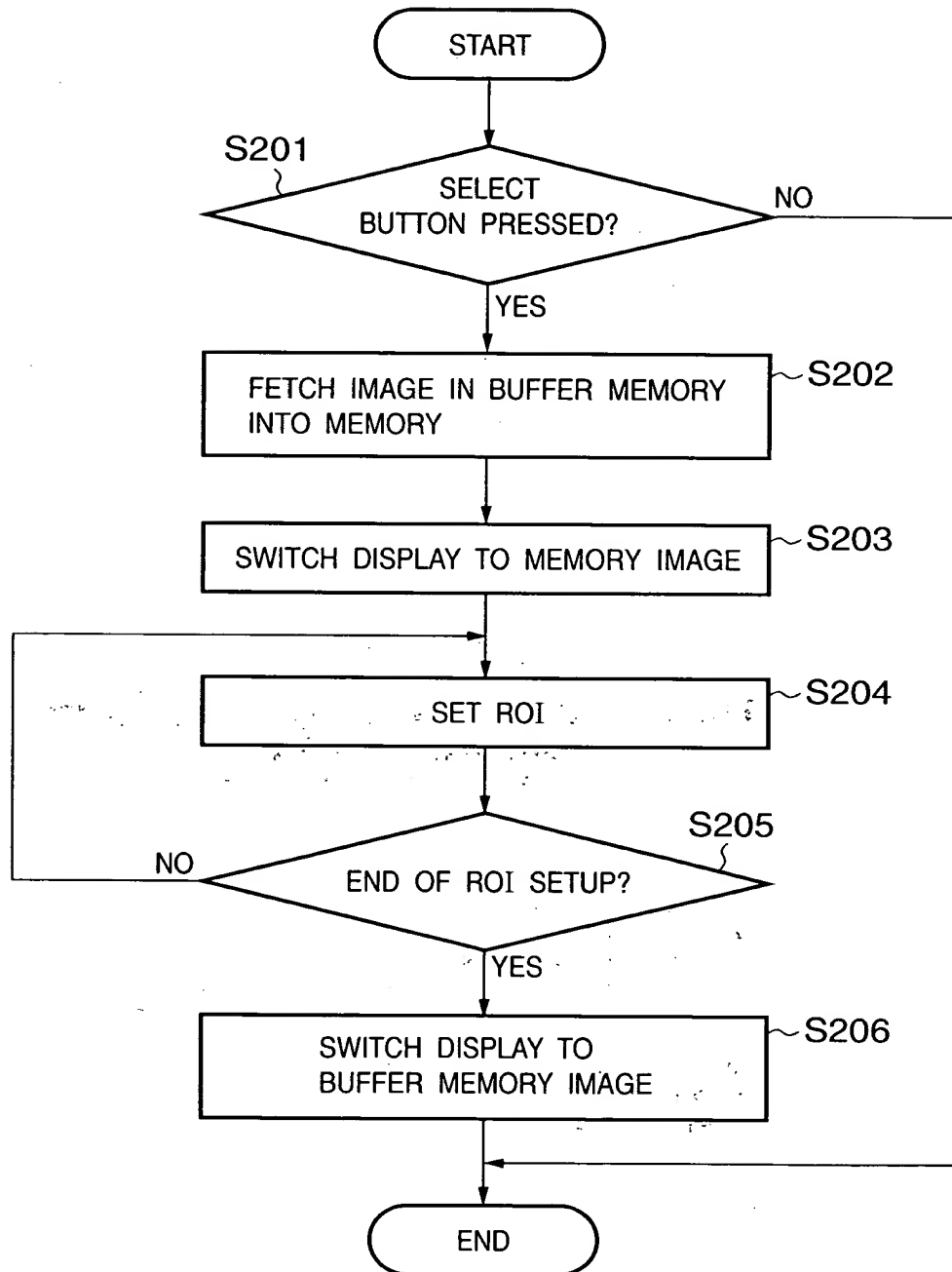


FIG. 23



T03290-10526860

FIG. 24

FIG. 24 is a block diagram of a video camera system. The system includes the following components and connections:

- Input/Control Section:**
 - 12 ZOOM** and **13 FOCUS** (represented by ovals) provide input to **15 CCD**.
 - 14** is a line connecting the input section to the processing section.
 - 16 CDS/AGC CIRCUIT**, **17 A/D CONVERSION CIRCUIT**, and **18 CAMERA SIGNAL PROCESSING CIRCUIT** are connected in series.
 - 19 BUFFER MEMORY** is connected to the signal processing circuit and the micro-computer.
 - 20 REPRODUCTION CIRCUIT** is connected to the buffer memory.
- Processing and Control Section:**
 - 21 COMPRESSION CIRCUIT** and **22 RECORDING CIRCUIT** are connected to the buffer memory.
 - 23 CAMERA MICRO-COMPUTER** is the central processing unit, connected to the buffer memory, recording circuit, and various motor drivers.
 - 24** is a line connecting the micro-computer to the system controller.
 - 25 IRIS MOTOR**, **26 IRIS MOTOR DRIVER**, **27 FOCUS MOTOR**, **28 FOCUS MOTOR DRIVER**, **29 ZOOM MOTOR**, and **30 ZOOM MOTOR DRIVER** are controlled by the micro-computer.
 - 31 ZOOM ENCODER** is connected to the zoom motor driver and the system controller.
- System Control and Output Section:**
 - 32 REGION DETECTION CIRCUIT** is connected to the buffer memory and the system controller.
 - 33 SYSTEM CONTROLLER** is the central control unit, connected to the micro-computer, region detection circuit, display control circuit, and cam table.
 - 34** is a line connecting the system controller to the cam table.
 - 35 TRIGGER** (represented by an oval) is connected to the system controller.
 - 36 REGION DESIGNATION LEVER** is connected to the system controller and the region designation lever detection circuit.
 - 37 REGION DESIGNATION LEVER DETECTION CIRCUIT** is connected to the region designation lever and the system controller.
 - 38 DISPLAY CONTROL CIRCUIT** is connected to the system controller and the display switching circuit.
 - 39 D/A CONVERSION CIRCUIT** is connected to the display control circuit and the monitor.
 - 40 MONITOR** is the output device.
 - 41 CAM TABLE** is connected to the system controller and the display control circuit.

FIG. 25

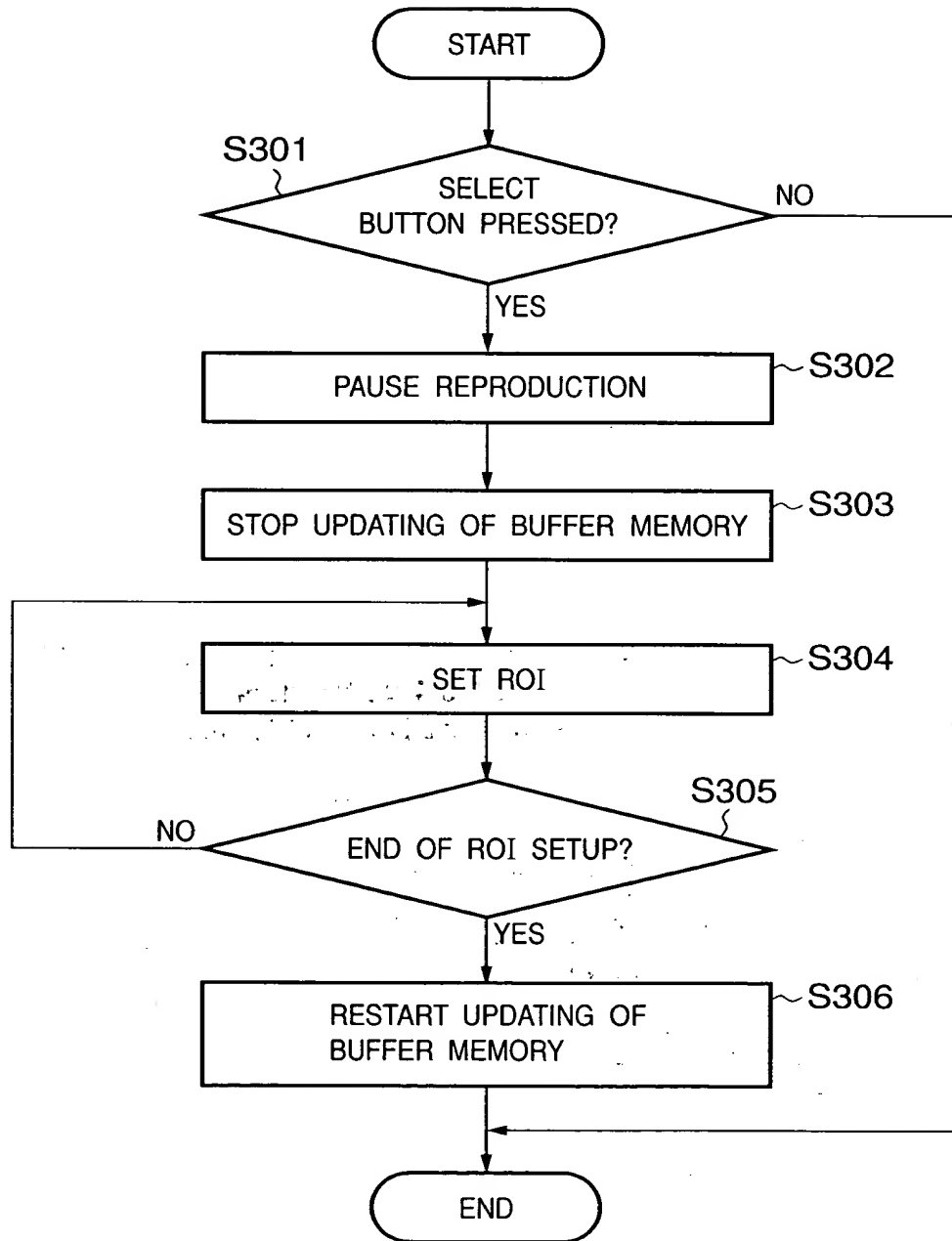


FIG. 26

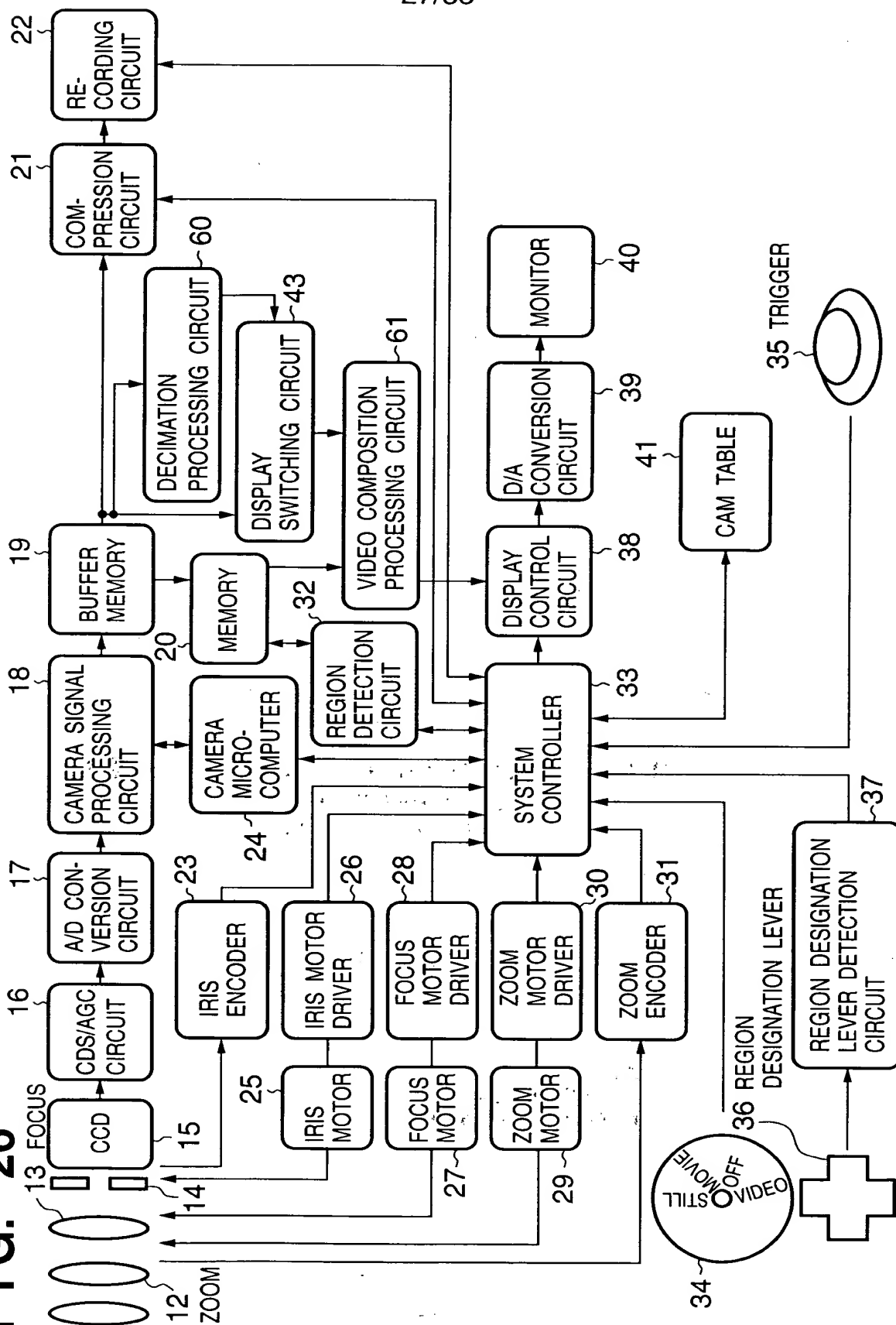
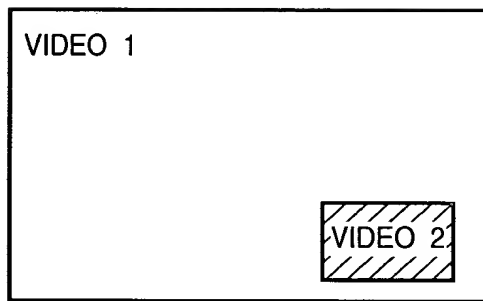


FIG. 27



FOB290-10526860

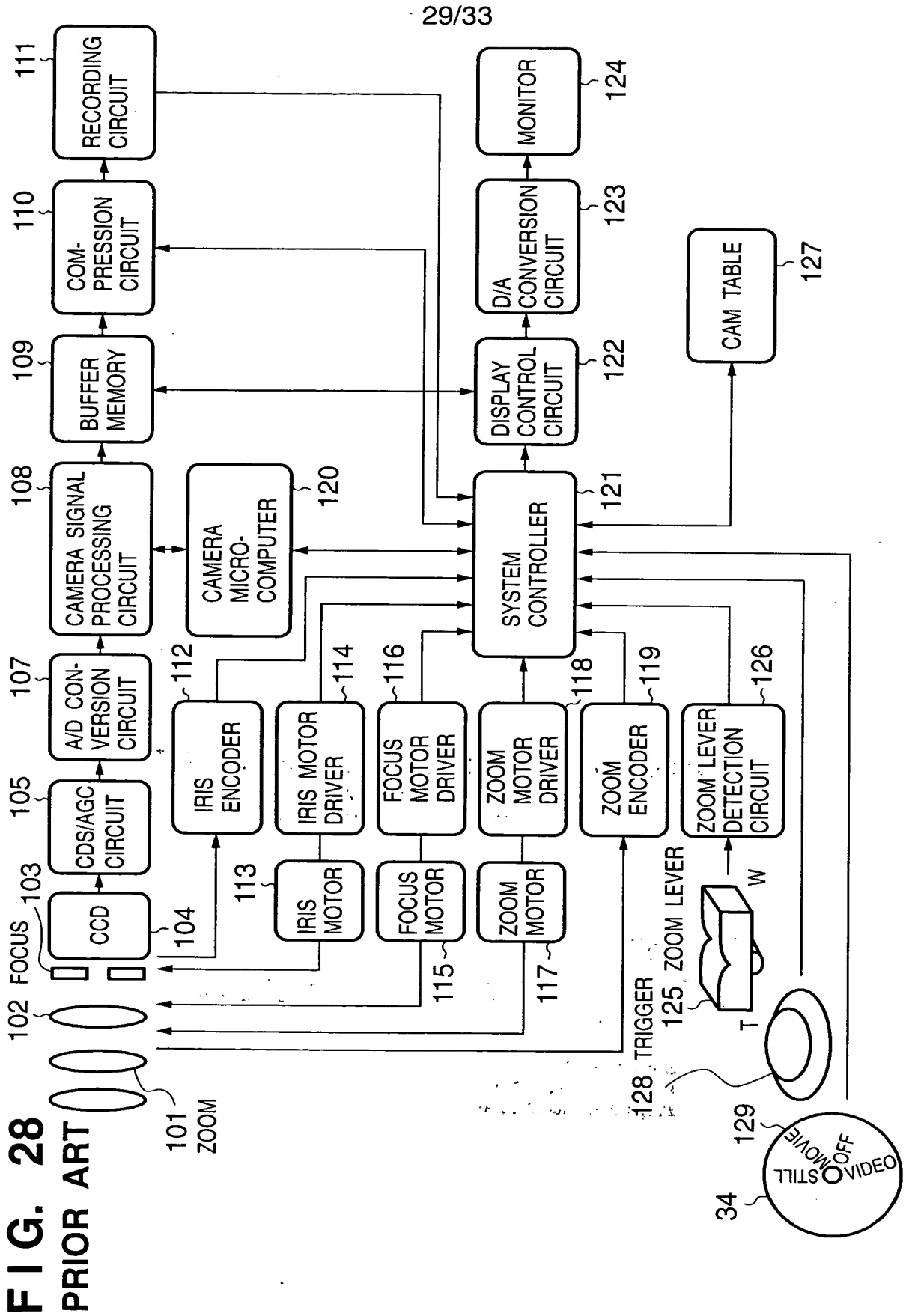


FIG. 29
PRIOR ART

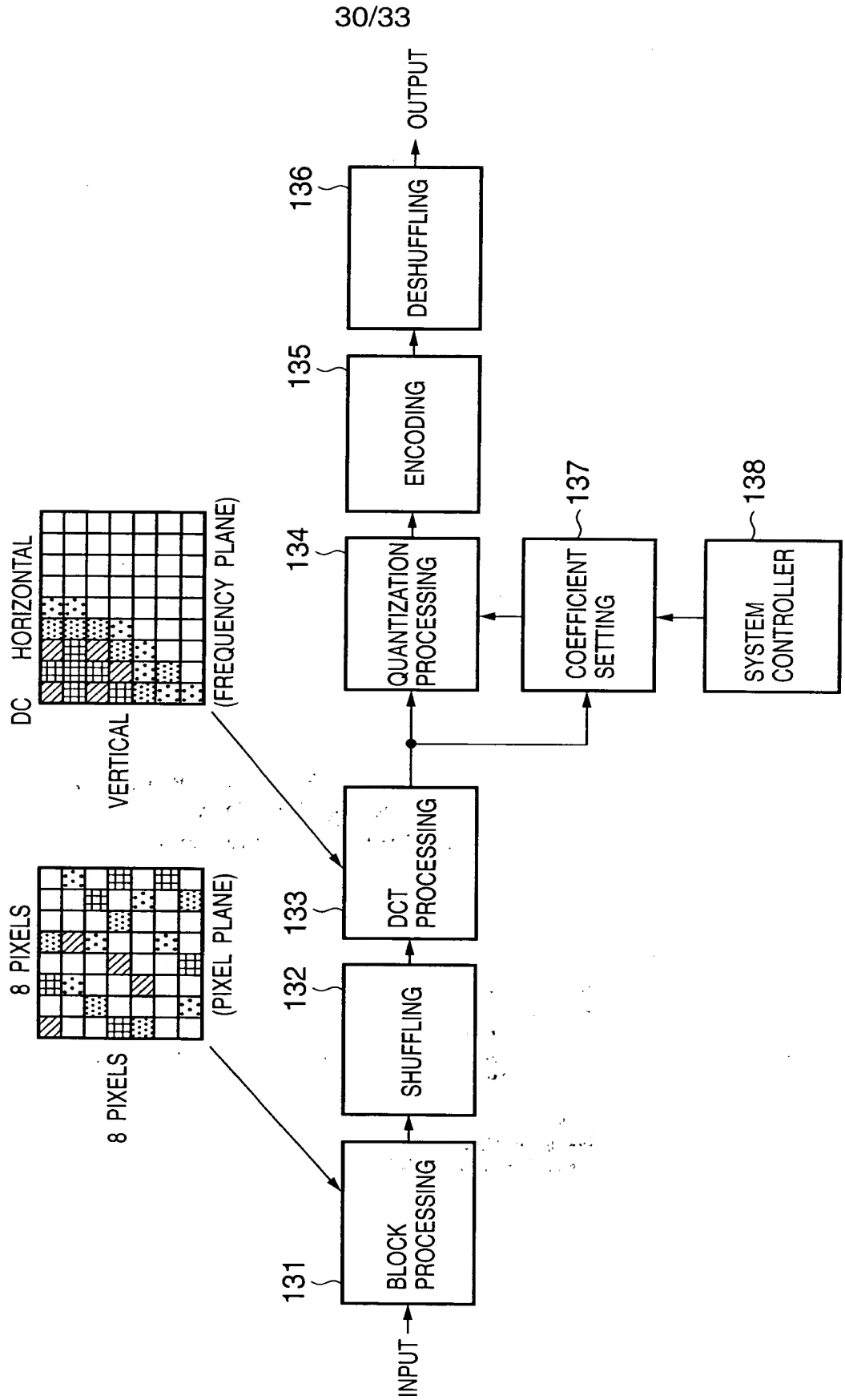


FIG. 30

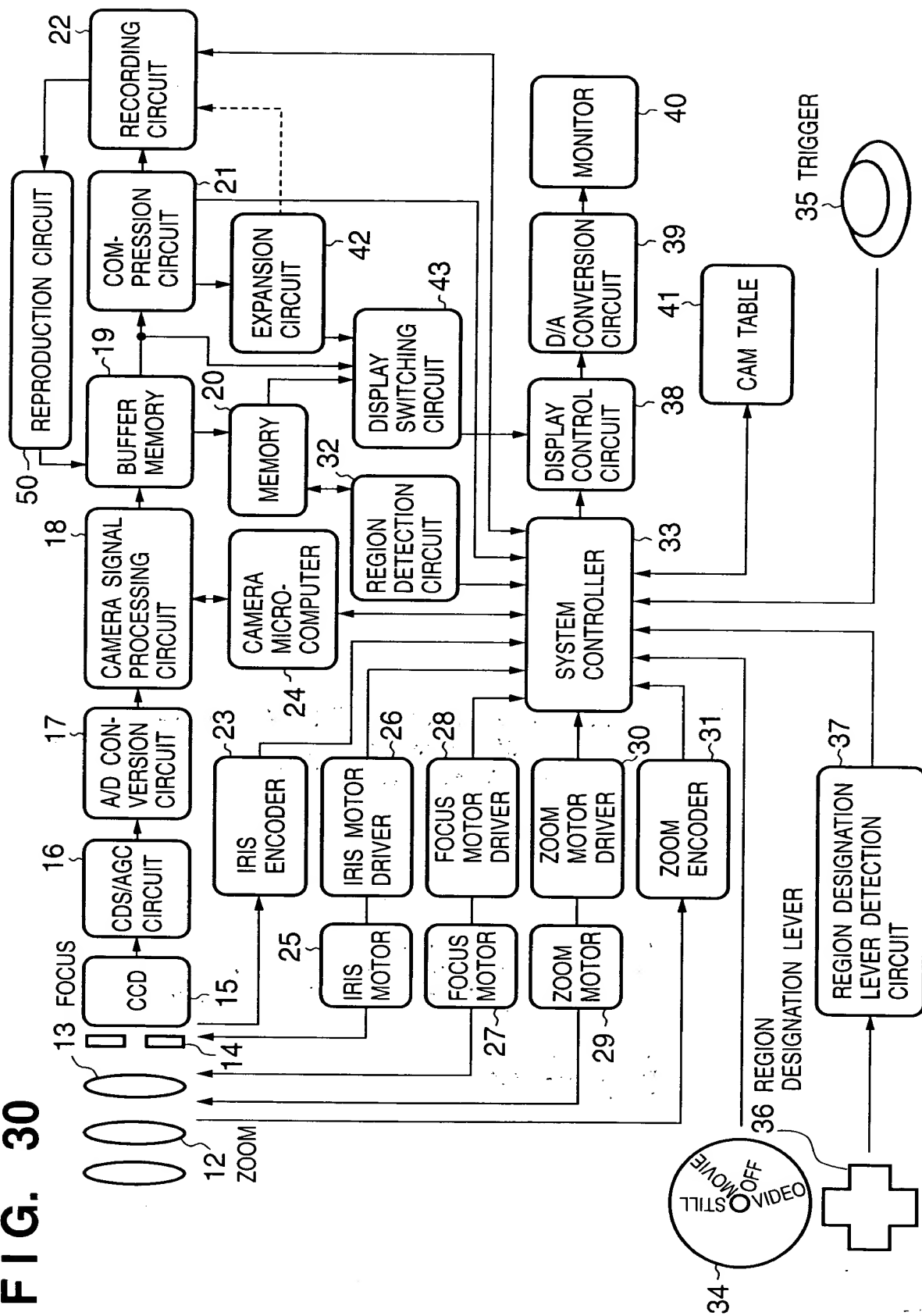


FIG. 31

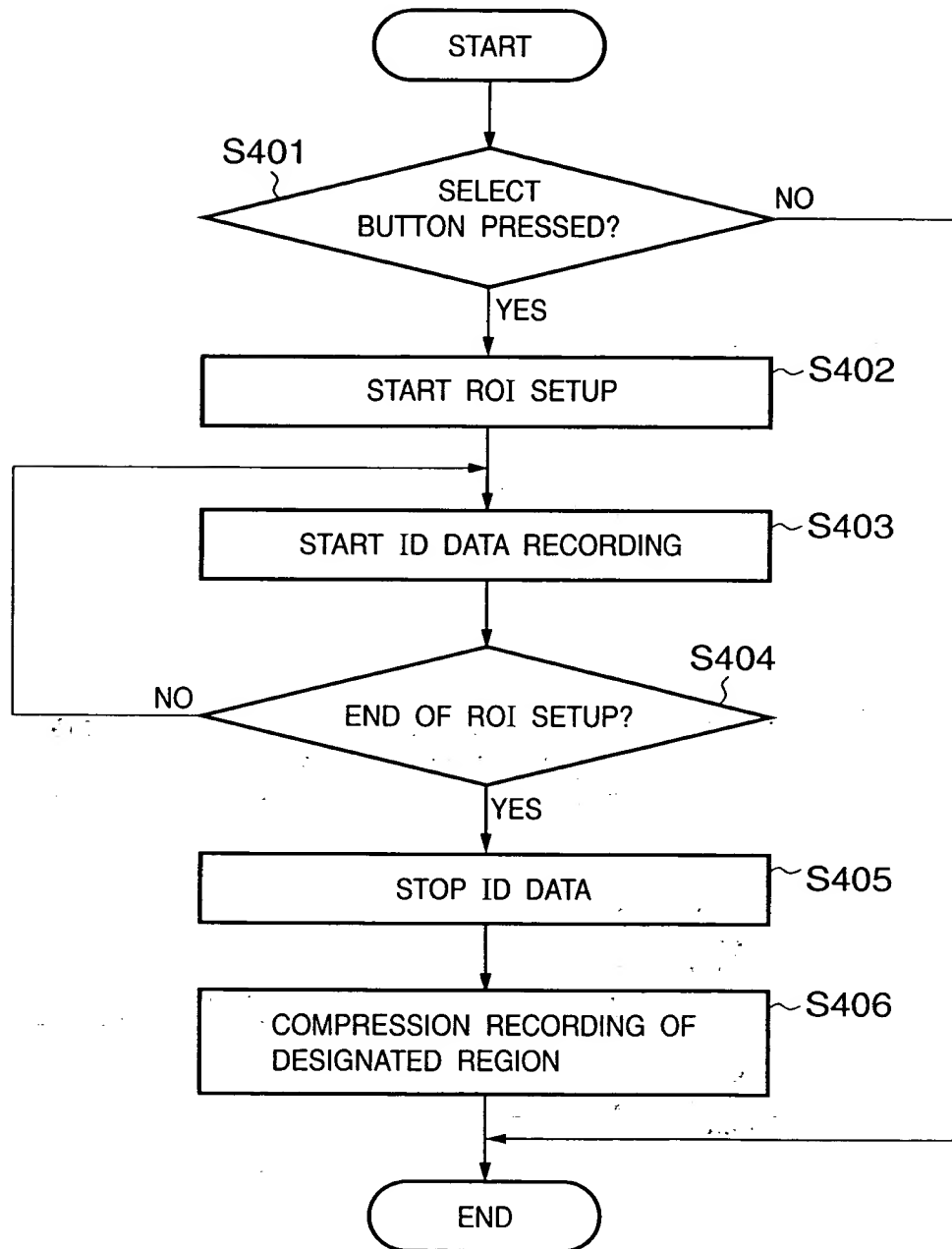


FIG. 32

